GateMate FPGA Technology

GateMate™ FPGA

new

Suitable from university projects up to high volume applications

Supported by:
Federal Ministry for Economic Affairs and Energy
on the basis of a decision by the German Bundestag

Overview

The GateMate™ FPGA family of Cologne Chip AG addresses all application requirements of small to medium size FPGAs. Logic capacity, power consumption, package size and PCB compatibility are best in class. GateMate™ FPGAs combine these features with lowest cost in industry making the devices well suited from University projects to high volume applications. Because of the outstanding circuit size/cost ratio, new applications now can use the benefits of FPGAs.

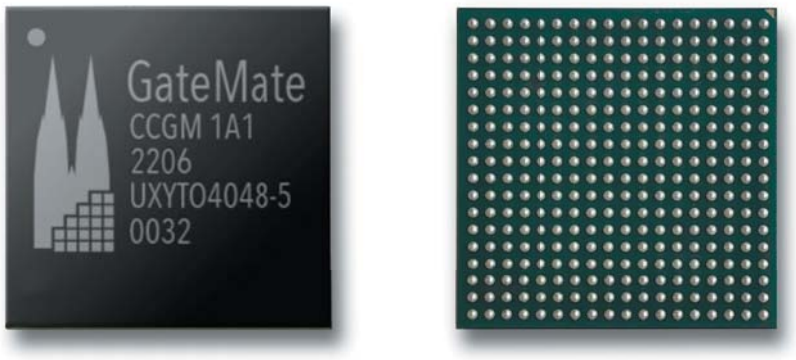
All this is based on a novel FPGA architecture combining Cologne Programmable Elements (CPE) with a smart routing engine. The CPE architecture allows an efficient building of arbitrarily-sized multipliers. Memory aware applications can use block RAMs with bit widths of 1 to 80 bits.

General Purpose IOs (GPIOs) can use different voltage levels from 1.2 to 2.5 Volt. All GPIOs can be configured as single-ended or LVDS differential pairs. Furthermore a high speed SerDes interface is available.

FPGA designs are synthesized using the Yosys framework. The Cologne Chip P&R software maps and implements the design into GateMate™ FPGA.

A Static Timing Analysis (STA) is also performed and gives evidence about critical paths and the overall performance of a design. The design can be simulated using Verilog netlist and SDF timing extraction.

The devices are manufactured using Globalfoundries™ 28 nm SLP (Super Low Power) process. Due to manufacturing in Europe, there is no danger of trade restrictions or high taxation.



FBGA 324 ball 15x15 mm with 0.8 mm ball pitch package of **GateMate™ CCGM1A1**

Cologne Chip
GateMate FPGA

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GateMate FPGA Technology

designed and manufactured in Germany

GateMate™ Features

- Logic capacity from 40.000 to more than a million LUT-4 equivalent cells
- DPSRAM 1.280 Mbit
- Novel architecture with new programmable element (CPE)
- CPE consists of LUT tree with 8 inputs
- 3 operation areas: low power, economy, speed
- FPGA in ball grid package for low size and high pin count
- Design conversion service free of charge for GateMate™ customers
- Only 2 signal layers on PCB necessary
- Low configuration bit count
- Very fast configuration using 4 bit SPI interface up to 100 MHz
- No excessive start-up currents
- Only two supply voltages needed, that can be applied in any order
- Multiple clocking schemas
- Dual-ported Block RAMs with 1-80 bits data width, also configurable as FIFO
- Multipliers with arbitrary factor sizes implementable
- SerDes 2.5 Gb/s
- General Purpose IOs (GPIO) configurable as single-ended or differential (LVDS)
- Pullup/Pulldown resistors configurable
- Support for ADC and DAC with additional IP cores
- Core voltage depending on application mode: 0.9 V, 1.0 V, 1.1 V
- Globalfoundries™ 28 nm SLP (Super Low Power) processMade in Europe
- Easy synthesis using the Yosys framework
- GateMate™ Place&Route with automatic clock Skew analysis and fixing
- Static Timing Analysis for performance evaluation
- Available in different size versions (see table)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	GND	VDD_WC	IO_NA_A0	IO_NA_A1	VDD_NA	IO_NA_A4	GND	IO_NA_A7	IO_NB_B0	GND	IO_NB_B2	IO_NB_B4	GND	IO_NB_B7	IO_EB_B8	VDD_EB	IO_EB_B5	GND	A
B	IO_WC_A8	IO_WC_B8	IO_NA_B0	IO_NA_B1	IO_NA_A2	IO_NA_B4	VDD_NA	IO_NA_B7	IO_NB_A0	VDD_NB	IO_NB_A2	IO_NB_A4	VDD_NB	IO_NB_A7	IO_EB_A8	GND	IO_EB_A5	VDD_EB	B
C	GND	VDD_WC	IO_WC_A7	IO_WC_B7	IO_NA_B2	IO_NA_A3	IO_NA_A5	IO_NA_A6	IO_NA_A8	IO_NB_B1	IO_NB_B3	IO_NB_B5	IO_NB_B6	IO_NB_B8	IO_EB_B7	IO_EB_B6	IO_EB_B4	IO_EB_A4	C
D	IO_WC_A5	IO_WC_B5	IO_WC_A6	IO_WC_B6	VDD_WC	IO_NA_B3	IO_NA_B5	IO_NA_B6	IO_NA_B8	IO_NB_A1	IO_NB_A3	IO_NB_A5	IO_NB_A6	IO_NB_A8	IO_EB_A7	IO_EB_A6	IO_EB_B2	IO_EB_A2	D
E	IO_WC_A3	IO_WC_B3	IO_WC_A4	IO_WC_B4	GND	VDD_NA	GND	VDD_NA	GND	VDD_NB	GND	VDD_NB	GND	VDD_EB	IO_EB_B3	IO_EB_A3	VDD_EB	GND	E
F	GND	VDD_WC	IO_WC_A2	IO_WC_B2	VDD_WC	GND	VDD_NA	GND	VDD	GND	VDD_NB	GND	VDD_EB	GND	IO_EB_B1	IO_EB_A1	IO_EB_B0	IO_EB_A0	F
G	IO_WC_A0	IO_WC_B0	IO_WC_A1	IO_WC_B1	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_EA	IO_EA_B8	IO_EA_A8	IO_EA_B7	IO_EA_A7	G
H	IO_WB_A7	IO_WB_B7	IO_WB_A8	IO_WB_B8	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B6	IO_EA_A6	VDD_EA	GND	H
J	GND	VDD_WB	IO_WB_A6	IO_WB_B6	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_EA	IO_EA_B5	IO_EA_A5	IO_EA_B4	IO_EA_A4	J
K	IO_WB_A5	IO_WB_B5	IO_WB_A4	IO_WB_B4	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B3	IO_EA_A3	IO_EA_B2	IO_EA_A2	K
L	IO_WB_A3	IO_WB_B3	IO_WB_A2	IO_WB_B2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_EA	IO_EA_B1	IO_EA_A1	VDD_EA	GND	L
M	GND	VDD_WB	IO_WB_A1	IO_WB_B1	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	IO_EA_B0	IO_EA_A0	GND	IO_SB_A3	IO_SB_B3	M
N	IO_WB_A0	IO_WB_B0	SPI_CS_N	SPI_CLK	VDD_WA	VDD	GND	VDD	GND	VDD	VDD_SB	GND	VDD_SB	IO_SB_A8	IO_SB_B8	N.C.	GND	VDD_SB	N
P	SPI_D1	SPI_D0	VDD_WA	GND	VDD_WA	VDD_SA	GND	VDD_SA	GND	VDD_SA	IO_SB_A4	IO_SB_A7	IO_SB_B7	IO_SB_A6	IO_SB_B6	VDD_PLL	IO_SB_A2	IO_SB_B2	P
R	SPI_D3	SPI_D2	JTAG_TCK	SPI_FWD	CFG_MD0	IO_SA_A1	IO_SA_A2	IO_SA_A4	IO_SA_A6	IO_SA_A7	IO_SB_B4	GND	IO_SB_A5	IO_SB_B5	VDD_SB	GND	IO_SB_A1	IO_SB_B1	R
T	VDD_WA	JTAG_TDI	JTAG_TMS	GND	CFG_MD1	IO_SA_B1	IO_SA_B2	IO_SA_B4	IO_SA_B6	IO_SA_B7	GND	SER_CLK	SER_CLK_N	VDD_CLK	RST_N	VDD_SER_PLL	GND	VDD_SB	T
U	POR_EN	JTAG_TDO	VDD_WA	CFG_MD2	IO_SA_A0	VDD_SA	IO_SA_A3	IO_SA_A5	VDD_SA	IO_SA_A8	SER_RX_P	VDD_SER	SER_TX_P	GND	GND	GND	IO_SB_A0	IO_SB_B0	U
V	GND	CFG_FAILED_N	CFG_DONE	CFG_MD3	IO_SA_B0	GND	IO_SA_B3	IO_SA_B5	GND	IO_SA_B8	SER_RX_N	SER_RTERM	SER_TX_N	GND	POR_ADJ	GND	VDD_SER	GND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Package Connections of **GateMate™ CCGM1A1** with ball positions and signal names

Device	Rel. size	Cologne Programmable Elements 1) 2)			Block RAM 3)		PLLs	SERDES	I/Os		Package	
		CPEs	8-Inp-LUT trees	FF/Latches	20Kb	40Kb			single-ended	differential	balls	size (mm)
CCGM1A1	1	20,480	20,480	40,960	64	32	4	1	162	81	324BGA	15x15
CCGM1A2	2	40,960	40,960	81,920	128	64	8	2	162	81	324BGA	15x15
CCGM1A4	4	81,920	81,920	163,840	256	128	16	4	154	77	324BGA	15x15
CCGM1A9	9	184,320	184,320	368,640	576	288	36	9	tbd	tbd	tbd	tbd
CCGM1A16	16	327,680	327,680	655,360	1,024	512	64	16	tbd	tbd	tbd	tbd
CCGM1A25	25	512,000	512,000	1,024,000	1,600	800	100	25	tbd	tbd	tbd	tbd

1) CPEs have 2x4 or 8 inputs connected to a LUT tree 2) Each CPE can be used as 2x2 Multiplier tile 3) Block RAM can have a data width of 1-80 bits

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