Low Power, High Performance, High Reliability

Arora FPGAs

Arora Family is designed to offer the best-in-class performance cost ratio FPGA. With abundant logic, high-performance DSP resources and high speed I/O, the family is optimized for co-processing to offload the application processor on intensive computation tasks. The Arora family is also the first FPGA with embedded pSRAM in the industry, which gives customers more usable device I/O.

LittleBee ® FPGAs

- Low Power Non-volatile FPGA
- Best in class of Performance Cost Ratio
- Small footprint
- MIPI standard supported
- Embedded pSRAM (GW1NR/1NSR only)

Based on 55nm LP technology, LittleBee® family offers instant-on, non-volatile, low power, intensive I/O and small footprint FPGA (smallest as 2.4x2.3mm). The family is ideal for high-performance bridging application and the
first FPGA that supports MIPI I3C and MIPI D-PHY standard in the industry. The LittleBee® family is also the first non-volatile FPGA with an embedded pSRAM in the industry, which further reduces the board space and enhances performance.

GoBridge ASSP

GoBridge ASSPs are highly integrated, low-power, single-chip devices for interfacing and communicating between various types of peripheal interfaces. The GoBridge ASSPs are ideal for converting from one type of peripheal interface to another, multiplexing between multiple interfaces or demultiplexing to multiple interfaces.

The first two devices in the GoBridge ASSP product line are the GWU2X and GWU2U ASSPs, which provide interface conversion between USB and SPI, JTAG, I2C, GPIO and UART. Future ASSP's will be added to the Gowin GoBridge product line soon.

Built-in Interface conversion processing and data buffering
I/O independent power supply, supports 3.3V, 2.5V, 1.8V level standards
Configurable register map
Independent clock adjustment
API provided in C/C++ for host device usage

GOWIN Education EDA

Gowin MCU Designer (GMD) education version is developed based on V1.0Beta, but you do not need to apply for license, and this version can only be used for education, research and other non-commercial purposes.

The released content of Gowin MCU Designer Education Edition includes:

· MCU core supported: ARM Cortex-M3
· Related Document: SUG549, Gowin MCU Designer User Guide

GOWIN EDA Home

GOWIN EDA (Gowin® EDA) – our easy to use integrated design environment provides design engineers one-stop solution from design entry to verification.

Features:

- Complete GUI based environment from FPGA design entry, code synthesis, place & route, bitsteam generation to download on the GOWIN FPGA on your boards.
- Integrates in-house Gowin Synthesis and 3rd-party Synplify Pro® from Synopsys® for front end design synthesis
- Supports creating RTL and Post-Synthesis.
    - RTL input files are RTL file complied with Hardware Description
- Language and constraints file that users require;
    - Post-synthesis input files are netlist file generated by user RTL
- Synthesis and constraints files that users require.
- Integrates IP Core Generator
- Online debug tool Gowin Analysis Oscilloscope (GAO) for instant analyze of signal design

Contact Wouter Pypen and schedule a live or virtual meeting to discuss how to find the best Gowin alternative FPGA for your hard to get Xilinx, Intel-Altera or Lattice FPGA's. Wouter is Alcom's FAE, manufacturer certified by Gowin.