The Benefits of Pseudo SLC (pSLC) Flash with Customizable Endurance

Single-level cell (SLC) NAND has always been the “golden standard” for industrial applications that require maximum reliability, performance and endurance. As its name implies, SLC is a type of NAND flash that stores only one bit of data per cell, so it has the advantage of faster write speeds and longer service life. Because SLC stores less data in each cell, storage devices based on this type of NAND flash cost higher and have lower capacities than those using other types. This translates to the highest cost per gigabyte among all flash types.

Data Storage Challenges

As the Industrial Internet of Things (IIoT), smart factories, autonomous vehicles and other data-intensive applications continue to gain traction, data storage requirements for such applications become more challenging. Organizations have to contend with infrastructure, security, diversity and data volume concerns, while considering the bottom line to make the most of their investments.

Due to the high cost of SLC flash, mission-critical industrial applications resort to using multi-level cell (MLC) or triple-level cell (TLC) flash to meet tight budgets when purchasing data storage devices. MLC stores two bits of data per cell while TLC stores three bits, allowing flash storage products to be available in higher densities and significantly lower costs than SLC. Advancements in controller design and the 3D NAND architecture have made it possible for MLC/TLC flash to become more reliable, but many applications still require higher levels of reliability and endurance balanced with higher usable densities.

Another pressing challenge is the diversity of use cases. Different workloads could require different assessment and drive configuration requirements for almost every customer. To save on purchase costs, some industries choose off-the-shelf solutions that may not fit the application-specific requirements.

Once deployed, they might easily wear out due to increased workloads, high program/erase (P/E) cycles, and extended temperatures. Low endurance, low tolerance to wide temperature ranges, and low reliability because of high error rates will eventually lead to more system down time, frequent component replacements and ultimately, higher costs.

A Closer Look at MLC/TLC NAND Flash

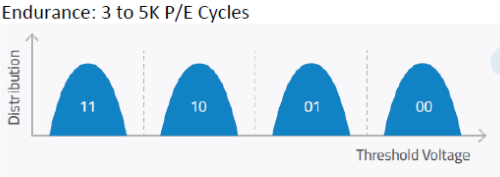
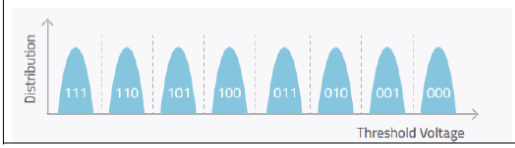
Why do MLC and TLC flash memories perform slower, have lower reliability and have shorter endurance?

SLC flash memory can hold one data bit, which allows the flash to have two states with a value of either 0 or 1. A cell is considered "programmed" or written to with a value of 0 and "erased" when it has a value of 1. Only one reference voltage is required to differentiate or distinguish between 0 and 1.

MLC stores two data bits of per cell, which allows the flash to have four states with values of 00, 01, 10, or 11. It takes two steps to program data on MLC; thus, the writing process is much slower than SLC. It takes three reference voltages to isolate the four states.

TLC stores three bits of data per cell, increasing the states to eight, with the values of 111, 011, 001, 101, 100, 000, 010 and 110 so the writing process is even slower than MLC's. It takes seven reference voltages to separate the eight states.

The following table compares the three NAND flash types.

Single-Level Cell (SLC) Stores 1 bit per cell Endurance: 50 to 100K P/E Cycles 	• High voltage margin makes cell reading easier and quicker • Small impact of leakage and cell interference • Wider distribution of logic levels means programming or erasing at lower voltage for increased durability and longer product lifetime.
Multi-Level Cell (MLC) Stores 2 bits per cell Endurance: 3 to 5K P/E Cycles 	• Lower cost per bit compared with SLC • Closer distribution means slight voltage shifts can generate more data errors and reduce product lifetime
Triple-Level Cell (TLC) Stores 3 bits per cell Endurance: ~ 1K P/E Cycles 	• Lower cost per bit compared with MLC • Very narrow voltage margin makes programming and reading speed very slow • Much closer distribution magnifies wear and significantly reduces product lifetime

** Theoretical estimate only. May vary depending on drive capacity, warranty period and program/erase cycles.*

Table 1. NAND Flash Types and Threshold Voltage (V_{th}) Distribution

To increase density in one memory chip, manufacturers employ "scaling," which involves shrinking cells to fit more in a die. Since MLC holds more data, cells in the array are closer. Every time data is written to a cell, voltage is applied to that cell. As more voltage is applied, the

programming operation affects, not only the V_{th} of that particular cell, but also of adjacent or surrounding cells. As temperature increases with the application of more voltage, electron leakage occurs. As a result, MLC wears out faster, altering the cells' original state, which in turn leads to errors when the cell is read, and memory cells interfering with each other's operations.

This phenomenon is called *program interference*, which affects surrounding cells and leading to errors. The error rate increases with each programming step. MLC controllers typically have powerful error correction algorithms, but it also takes time to guarantee accuracy, resulting in slower throughput.

A related occurrence arising from the scaling down of memory cells is *read disturbance*. When a row of cells is read, it impacts the threshold voltage of the surrounding unread cells, alters their logical states, and leads to read errors that impact flash endurance.

Pseudo SLC: The Golden Mean

For mission-critical applications where reliability and long usage life are essential, SLC is ideal but its cost is prohibitive, and capacities may be too low for some applications. MLC and TLC offer higher capacities and are more cost-friendly, but some applications require higher reliability and endurance. Could there be a middle ground or "golden mean" that could offer the best of both worlds, offering superior performance, durability and reliability at ample capacities and more accessible price points?

The answer is "Yes," and it is called pseudo SLC (pSLC), which also goes by several marketing names such as enhanced MLC, superMLC, iSLC, advanced MLC (aMLC). The main idea is to make MLC/TLC function like SLC by storing only one data bit per cell instead of two or three.

ATP Electronics' Premium Line: 3D TLC SSDs Configured as pSLC with Customizable Endurance

ATP recently launched the A700Pi/E700Pi Series, a new generation of Premium Line pSLC NAND-based embedded SSDs. These SSDs use advanced controller and firmware technologies to make sure that the offerings meet and even exceed the endurance requirements of demanding applications.

By offering the best balance between SLC and TLC, ATP's pSLC-based embedded SSDs offer the best total cost of ownership (TCO) value for cost in terms of endurance, as measured in terabytes written (TBW) and drive writes per day (DWPD).

A game-changing highlight for this generation is a new ATP-developed firmware and supporting mass production infrastructure, which are fully customizable to endurance configurations that are tailor-fitted to customer's requirements, to address any variety of embedded/industrial usage cases. This once again demonstrates ATP's commitment to deliver optimal total cost of ownership (TCO) value for its customers as storage demands of the Industrial Internet of Things (IIoT), edge computing, and other high-reliability applications continue on the upsurge.

The succeeding paragraphs provide more details on the endurance benefits and configurations of the new A700Pi/E700Pi Series. If customers need special endurance specifications beyond what is specified in this article, they are welcome to inquire and discuss their requirements with ATP sales representatives in their area.

The following table shows the advantages of the A700Pi/E700Pi Series.

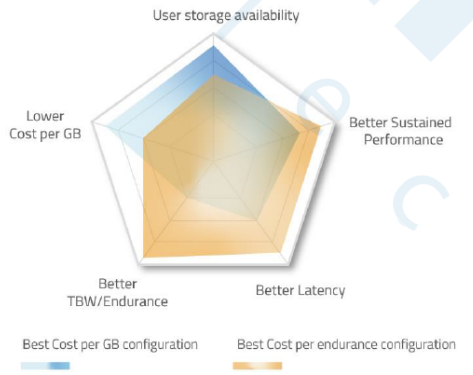
ATP pseudo SLC (pSLC) TLC flash that stores 1 bit per cell instead of 3 	• Purpose-built for applications that require uncompromising endurance at lower user capacities. • Reduces the capacity but extends the general endurance to more than 10X of the same TLC products. • Dramatically improves the sustained write performance and reliability of the drives, making them suitable for write-intensive applications. • Drive down TCO with longer service life using the most cost-effective NAND flash technology available.

Table 2. ATP's Customizable Premium Line with 3D TLC NAND flash configured as pSLC offers a balance in usable density at a better price point (Cost per GB), and impressive improvements in reliability, sustained performance, and endurance (Cost per TBW), which all boil down to best TCO value.

The following graph shows the new customizable pSLC-configured SATA III SSDs demonstrating significant improvements in endurance compared with default 3D TLC offerings.

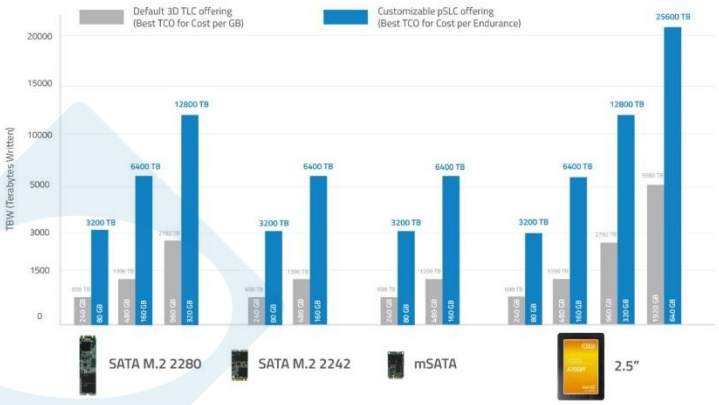


Figure 1. Comparison of endurance ratings between default 3D TLC offerings and ATP's new customizable pSLC-configured SATA SSDs.

ATP's new Premium Line is available in both raw and managed NAND. Key specifications are provided in the succeeding table.

Flash Mode	Pseudo SLC (pSLC)					3D TLC					Pseudo SLC (pSLC)		3D MLC & TLC	
Product name	A700Pi					A600Pi					E700Pi		E600Si	
Interface/ Form Factor	SATA III										e.MMC			
Operating Temperature	-40°C to 85°C										-40°C to 85°C			
Form factor		M.2 2280	M.2 2242	mSATA	2.5"		M.2 2280	M.2 2242	mSATA	2.5"	153-ball FBGA			
Capacity	Max. Endurance*					Max. Endurance*					Max. Endurance*		Max. Endurance*	
	80 GB	3,200 TB				240 GB	698 TB				21 GB	296 TB	64 GB (TLC)	27 TB
	160 GB	6,400 TB				480 GB	1,396 TB				64 GB	1,320 TB	64 GB (MLC)	412 TB
	320 GB	12,800 TB			12,800 TB	960 GB	2,792 TB						128 GB (MLC)	824 TB
	640 GB				25,600 TB	1920 GB				5,585 TB				

*Under highest Sequential write value. May vary by density, configuration and applications